REMARKS

Claims 1-10 and 25-44 remain pending in this application. Claims 1-4, 9, 10, 25-28, 33-38, 43 and 44 are rejected. Claims 5-8, 29-32 and 39-42 are objected to.

In the present Office Action the Examiner indicated that the RCE and Preliminary Amendment filed on April 24, 2006 have been entered. Applicants acknowledge that the Examiner has withdrawn the rejection over ***Manning*** in light of the arguments presented in the amendment filed April 24, 2006. Additionally, the Examiner indicated that claims 5-8, 29-32 and 39-42 contain allowable subject matter.

Claims 1-4, 9-10, 35-38 and 43-44 are rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,483,359 (***Lee***) in view of U.S. Patent No. 5,101,117 (***Johnson).*** Applicant respectfully traverses this rejection.

Applicants respectfully assert that the combination of ***Lee*** and ***Johnson*** does not teach, disclose or make obvious all of the elements of claim 1 of the present invention. Applicants respectfully assert that all of the elements of independent claims 1 and 35 (both as amended) are not taught, disclosed, or suggested by ***Lee***. The Examiner merely listed a few elements, such as a phase detector, a first delay line and a second delay line and a feedback line of ***Lee*** to assert anticipation of claims 1 and 35. The Examiner merely provides conclusory statements equating the delay lines of ***Lee*** to the course delay circuit and the fine delay called for by claims of the present invention. In other words, the Examiner merely lists various reference numbers next to certain words out of the elements of claims of the present invention. ***Johnson*** does not make for this deficit. Applicants respectfully assert that ***Lee*** and ***Johnson*** does not teach, disclose or suggest all of the elements of claims 1 and 35 of the present invention.

The Examiner uses the capacitors (capacitor 60 of Figure 3 and capacitors 72a-72l of Figure 4) of ***Johnson*** and the capacitors C1, C2, C3, in Figures 4, and 6A through 6D of ***Lee*** to argue anticipation of elements of the claims of the present invention. However, Applicant respectfully asserts that claim 1 and 35 of the present invention call for a delay lock loop that comprises a delay circuit for activating a transistive capacitive delay. In contrast, the disclosure of ***Lee*** merely refers to a passive capacitor that may be connected to the inverted clock signal, as described in Figures 4 and 6A-6D of ***Lee***. Further, ***Johnson*** doesn't make up for this deficit. The Examiner provides no explanation or arguments as to how the disclosure of ***Lee*** anticipates elements of claims of the present invention. Further, ***Lee*** simply does not disclose a transistive capacitive delay, as called for by claims 1 and 35 of the present invention. Various advantages of implementing the present invention is achieved over the prior art. For example, the Specification discloses the issue of an RC time constant that may become problematic when applying the standard passive capacitor, as disclosed by ***Lee***. Further, utilizing the transistive capacitive elements, an advantage of providing for a relatively constant capacitance during voltage transitions may be achieved, which is a feature that is not provided by ***Lee***. *See* Specification, p.19, lines 3-15. Therefore, various exemplary advantages may be achieved utilizing the transistive capacitive disclosed by claims 1 and 35. ***Lee*** simply does not disclose activating a transistive capacitive delay, as called for claims 1 and 35 of the present invention. Therefore, ***Lee*** clearly does not anticipate all of the elements of claims 1 and 35 of the present invention.

The Examiner attempts to make up for the deficit of ***Lee*** by adding the disclosure of ***Johnson*** to make obvious the transistor capacitor delay. Aside from being non-analogous art, ***Johnson*** does not make up for the deficits of ***Lee***. ***Johnson*** is merely directed to a system for

synchronizing the operation of a CPU and a co-processor. ***Johnson*** discloses a FPC chip 20 capable of accessing system data-bus in order to synchronize the data access. *See* column 3, lines 1-5. ***Johnson*** discloses a phase detector that supplies an output indicative of the phase difference of the signals received on line 18, which is a CPU output enable signal and on line 19, which an FPC output enable signal. *See* column 3, lines 5-8. Therefore, the phase detector of ***Johnson*** is not directed towards data transfer, it is directed towards enabling two different entities. ***Johnson*** does not disclose a feedback signal for using the phase detector. Therefore, ***Johnson*** is entirely different and non-analogous to ***Lee*** and those skilled in the art would not be motivated to combine them to make obvious all of the elements of claims of the present invention.

The present invention calls for detecting the phase difference between a reference signal and a feedback signal and then using a delay circuit for activating a transistive capacitive delay. These are elements that are not disclosed or suggested by either ***Lee*** or ***Johnson***, or a combination of the two. ***Johnson*** does not disclose or make obvious transistive capacitances. The Examiner incorrectly identifies the capacitors 72a-72l in Figure 4 as a transistive capacitor. The Examiner is false in this assertion. The capacitors shown in Figure 4 (72a-72l) are actually simple passive capacitors whose connection is influenced by the transistors 71a-71l. *See* Figure 4 of ***Johnson***. ***Johnson*** clearly discloses that the delay line in Figure 4 consists of a series of drivers and control transistors 71a-71l and 12 capacitors 72a-72l. *See,* column 4, lines 39-44. Therefore, neither ***Lee*** nor ***Johnson*** discloses or makes obvious a transistive capacitor. Similarly, the Examiner's citation of the capacitor 60 in Figure 3 of ***Johnson*** is also similarly false since the capacitor 60 is simply a passive capacitor. Therefore, ***Johnson*** also has all of the

weaknesses of ***Lee*** and the combination of ***Johnson*** and ***Lee*** do not teach, disclose or suggest all of the elements of the claims of the present invention.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. As described above, the combination of ***Lee*** and ***Johnson*** do not teach or suggest all of the elements of claims 1 and 35 of the present invention.

Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Applicant respectfully asserts that the Examiner has provided no evidence, nor is there any evidence in the cited prior art that would provide an indication of motivation of those skilled in the art to combine ***Lee*** and ***Johnson*** to read upon all of the elements of claims 1 and 35of the present invention. Contrary to the Examiner's contention, those skilled in the art simply would not find motivation to combine ***Johnson*** and ***Lee***. The Examiner stated that those skilled in the art would combine ***Johnson*** and ***Lee*** for the purpose of reducing size by employing the transistive capacitor. There are two flaws in this reasoning. First, neither ***Johnson*** nor ***Lee*** discloses transistive capacitors. Secondly, reduction of size is not a motivation to use the transistive capacitor, there are other motivations exemplified above, such as the advantage of providing a relatively constant capacitance during voltage transitions. These are motivations that are not addressed or anticipated by ***Lee*** nor ***Johnson***. Without improper hindsight, those skilled in the art simply would not find the motivation to combine the delay lock loop of ***Lee*** with the data path disclosure of ***Johnson*** to make obvious all of the elements of claims 1 and 35. Therefore, there is no evidence or motivation, either in the references

themselves or in the knowledge, generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. There is no evidence that the improbable combination of ***Lee*** and ***Johnson*** provide a reasonable expectation of success. There is no evidence to a contrary assertion, and the Examiner fails to provide any evidence of reasonable expectation of success based upon the prior art. Therefore, the Examiner failed to establish a *prima facie* evidence of obviousness with respect to claims 1 and 35 of the present invention. Accordingly, for a least the reasons described above ***Lee*** and ***Johnson*** do not cause all of the elements of claims 1 and 35 to be are taught, disclosed, or suggested. The Examiner failed to show a *prima facie* case of obviousness of claims 1 and 35. Accordingly, independent claims 1 and 35 are allowable. Further, dependent claims 1-4, 9-10 which depend from claims 1, and claims 36-38, 43-44, which depend from claim 35, are also allowable for at least the reasons cited herein.

Claims 1-4, 9-10, 25-28, 33-38 and 43-44 are rejected under 35 USC 103(a) as being unpatentable over ***Baker*** (US 6,445,231) in view of ***Lee*** (US 6,483,359). Applicants respectfully traverse this rejection.

As described above, ***Lee*** clearly does not disclose many of the elements of claim 1 of the present invention. The inclusion of ***Johnson*** and ***Baker*** does not make up for this deficit. The Examiner stated that ***Baker*** does not disclose the DLL circuit comprising delay circuit as recited in claims 1, 25 (as amended), and 35. The Examiner then uses ***Lee*** and ***Johnson*** to make up for

this deficit. However, ***Baker*** clearly does not disclose the delay circuit at all, much less a delay circuit for activating a transitive capacitor delay. As described above, neither ***Lee*** nor ***Johnson*** disclose a delay circuit for activating a transitive capacitor delay. Therefore, the combination of ***Baker***, ***Lee*** and ***Johnson***, does not teach, disclose or suggest all of the elements of claim 1 of the present invention. Hence, the first prong of showing a *prima facie* obviousness is not shown.

Further, those skilled in the art would not combine ***Baker*** with ***Lee*** and/or ***Johnson*** to make obvious all of the elements of claim 1 of the present invention. Simply because ***Lee*** and ***Johnson*** disclose a DLL loop, the Examiner failed to provide any evidence motivation why those skilled in the art would combine them to make obvious the elements of claim 1, 25, and 35 of the present invention, particularly, the delay circuit for activating a transitive capacitive delay. Nothing in ***Lee*** discloses or suggests that those skilled in the art would look for a solution for the transitive capacitor delay and attempt to combine any prior art cited. Hence, the second prong of showing a *prima facie* obviousness is not shown.

Additionally, there is no evidence that the improbable combination of ***Baker***, ***Lee*** and ***Johnson*** provide a reasonable expectation of success. There is no evidence to a contrary assertion, and the Examiner fails to provide any evidence of reasonable expectation of success based upon the prior art. Hence, the third prong of showing a *prima facie* obviousness is not shown. However, as described above, even if all of the cited prior art were combined, all of the elements of claims 1, 25, and 35 of the present invention would not be taught, disclosed or suggested. As described above, the Examiner failed to provide a *prima facie* showing of obviousness of claims 1, 25, and 35. Therefore, independent claims 1, 25, and 35 of the present invention are allowable for at least the reasons cited herein. Further dependent claims 1-4, 9-10,

which depends from claim 1; claims 26-28, 33-34, which depends from claim 25; and claims 36-38, 43-44, depends from claim 35 is also allowable for at least the reasons cited herein.

Applicants acknowledge and appreciate that the Examiner has indicated that claims 5-8, 29-32 and 39-41 contain allowable subject matter; however, in light of the arguments presented herein, all pending claims of the present invention are allowable. Therefore, Applicant respectfully solicits a Notice of Allowance, allowing claims 1-10 and 25-44 of the present invention.

In light of the arguments presented above, Applicants respectfully assert that claims are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, **the Examiner is requested to call the undersigned attorney** at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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